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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,110	01/23/2004	William C. Moyer	SC13158TH	7889

23125 7590 12/09/2004

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EXAMINER	
IQBAL, NADEEM	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,110	MOYER, WILLIAM C.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-35 and 46-48* is/are allowed.

6)☐ Claim(s) *1-5,10,12 and 36* is/are rejected.

7)☐ Claim(s) *6-9,11,13-21 and 37-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Jan 23, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5, 10, 12, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagen, (U.S. Patent number 6816924) in view of Dokie et al., (U.S. Patent number 6145007).

4. As per claims 1 & 36, Hagen teaches (col. 2, lines 32-35) a DMA controller that supervises bus handling, the DMA controller includes a priority controller, a bus sniffer, and a context machine. .The buss sniffer and context machine identify block transfers as frame or cell transfers. He thus teaches limitations pertain to a system comprising, a communication bus, a DMA device coupled to the bus, direct memory device controlling channels of information. He also teaches (col. 2, lines 41-45) a trace and debug support unit that works in conjunction with

the bus sniffer. He thus teaches a debug control circuitry coupled to the DMA device. He does not explicitly disclose that the debug control circuitry providing debug messages that identify an existence of a DMA channel transfer boundary for at least one predetermined channel. Dokie et al., (Dokie) teaches (col. 2, lines 20-22) a method for providing exchange of messages between first and second processors and further teaches (col. 5, lines 23-25) interprocessor communication registers support a control messaging protocol for communication between processing cores. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Hagen to include the interprocessor communication support for control messaging protocol to provide communication between processors. This is because Dokie also teaches (col. 5, lines 38-40) Debug circuitry to assist in application development and system debug, and also teaches (col. 2, lines 33-35) that the principles of his invention can be utilized in the design and operation of systems such as processing streaming data, and where accurate and high speed throughput are essential, thus provides motivation for the stated inclusion.

5. As per claim 2, Hagen teaches (col. 2, lines 33-35) that the DMA controller includes a priority controller, a bus sniffer and a context machine, and the bus sniffer and context machine identifies block transfers as frame or cell transfers and supervise interleaving. He thus teaches limitations pertain to programmable control means for selecting which of the channels of information controlled by the direct memory access device that the debug messages will identify the channel transfer boundaries.

6. As per claim 3, Dokie teaches (col. 5, lines 23-25)) interprocessor communication registers support a control messaging protocol for communication between processing cores. He

thus provides debug messages to indicate that a channel transfer has started for the at least one predetermined channel with the inclusion with the invention of Hagen, since Dokie teaches a control messaging protocol for communication between processing cores.

7. As per claim 4, Dokie also teaches (col. 6, lines 50-52) Static debugging that involves halting the system and altering/viewing the states of the various sub-systems via their control/status registers.

8. As per claim 5, Dokie teaches as stated above that Static debugging that involves halting the system and altering/viewing the states of the various sub-systems via their control/status registers. Therefore would also allow for viewing states for status parameters as channel priority, utilization factor and whether a transfer error has occurred, as claimed.

9. As per claim 10, Dokie teaches as stated above that Static debugging that involves halting the system and altering/viewing the states of the various sub-systems via their control/status registers. Therefore would also allow for indication of periodic of the at least one predetermined channel.

10. As per claim 12, Hagen substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 2, lines 32-35) a DMA controller that supervises bus handling, the DMA controller includes a priority controller, a bus sniffer, and a context machine. .The buss sniffer and context machine identify block transfers as frame or cell transfers. He thus teaches limitations pertain to a system comprising, a communication bus, a DMA device coupled to the bus, direct memory device controlling channels of information. He also teaches (col. 2, lines 41-45) a trace and debug support unit that works in conjunction with the bus sniffer. He thus teaches a debug control circuitry coupled to the DMA device. He does not explicitly

discloses that the debug control circuitry providing debug messages that periodically provide at least one status parameter for at least one predetermined channel. Dokie et al., (Dokie) teaches (col. 2, lines 20-22) a method for providing exchange of messages between first and second processors and further teaches (col. 5, lines 23-25) interprocessor communication registers support a control messaging protocol for communication between processing cores. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Hagen to include the interprocessor communication support for control messaging protocol to provide communication between processors. This is because Dokie also teaches (col. 5, lines 38-40) Debug circuitry to assist in application development and system debug, and also teaches (col. 2, lines 33-35) that the principles of his invention can be utilized in the design and operation of systems such as processing streaming data, and where accurate and high speed throughput are essential, thus provides motivation for the stated inclusion.

Allowable Subject Matter

11. Claims 22-35, 46-48 are allowed.

12. Claims 6-9, 11, 13-21, 37-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI